



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#3  
11-7-97

Application of:  
Mailloux, et al.

Serial No.: 08/650,719

Filed: May 20, 1996

For: BURST/PIPELINED EDO MEMORY DEVICE

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§ Group Art Unit: 2318  
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§ Examiner: Peikari, B. J.  
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§ Atty. Docket: 95-0653  
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§ Paper No. 2  
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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

Certificate of Mailing (37 C.F.R. § 1.8)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:

10/31/97 Date  
Peggy Lloyd Signature

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant[s] respectfully request[s] that this Information Disclosure Statement be entered and that the references listed on the attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed references are enclosed for the convenience of the Examiner.

In accordance with 37 C.F.R. § 1.97(b), this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possible material information as defined in 37 C.F.R. § 1.56(a) exists.

The following references are submitted for the Examiner's review:

U.S. Patents

<u>U.S. Patent No.</u>	<u>Issue Date</u>	<u>Inventor</u>
5,357,469	10/18/94	Sommer et al.
5,268,865	12/7/93	Takasugi
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Toshiba America Electronic Components, Inc., "4M DRAM 1991", Pgs. A-137 - A-159

Micron Semiconductor, Inc., "1994 DRAM Data Book", pgs. 2-1 to 2-6

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Toshiba Corp., "Integrated Circuit Technical Data-262,144 Words x 8 Bits Multiport DRAM", TC52826TS/Z/FT/TR-1, TEN. Rev. 2.1

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Dave Bursky, "Novel I/O Options and Innovative Architectures Let DRAMs Achieve SRAM

Performance; Fast DRAMS can be swapped for SRAM Caches", Electronic Design, Vol. 41, No. 15, Cleveland, Ohio, pp. 55-67, (July 22, 1993)

Shiva P. Gowni, et al., "A 9NS, 32K X 9, BICMOS TTL Synchronous Cache RAM With Burst Mode

Access", IEEE, Cutsom Integrated Circuits Conference, pp. 781-786, (March 3, 1992) S3 Incorporated, "S3 Burst Mode DRAM", 6/93, 2 pages

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This Information disclosure Statement is being submitted after the mailing of the first Office Action, but before the mailing of a Final Rejection or Notice of Allowance. The Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) of \$240.00 and any additional fees which may be required to Micron Technology, Inc. Deposit Account No. 13-3092, Order No. 97-0242.00.

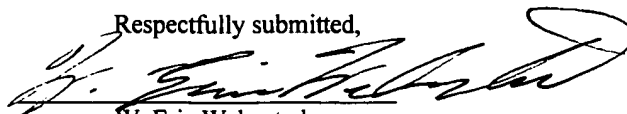
If there are any matters which may be resolved or clarified through telephone interview, the Examiner is respectfully requested to contact Applicant's undersigned attorney at the number indicated.

\* \* \* \*

A Form PTO-1449 is enclosed herewith.

Date: 10-30-97

Respectfully submitted,



W. Eric Webostad  
Reg. No. 35,406  
Micron Technology, Inc.  
8000 S. Federal Way  
Boise, ID 83706-9632  
(208) 368-4792